TIGER ELECTRONICO.,LTD

LM4890

1 WATT AUDIO POWER AMPLIFIER

General Description

The LM4890 is an audio power amplifier primarily designed for demanding applications in mobile phones and ther portable communication device applications. It is capable of delivering 1 watt of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) from a 5VDC power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4890 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consum-

ption is a primary requirement.

The LM4890 features a low-power consumption shutdown mode, which is achieved by driving the shutdown pin with logic low. Additionally, the LM4890 features an internal thermal shutdown protection mechanism. The LM-

4890 contains advanced pop & click circuitry which eliminates noises which would otherwise occur during turn-on and turn-off transitions.The LM4890 is unity-gain stable and can be configured by external gain-setting resistors.

Key Specifications

- ◆ PSRR at 217Hz, VDD = 5V (Fig. 1) 62dB(typ.)
- ◆ Power Output at 5.0V & 1% THD 1W(typ.)
- ◆ Power Output at 3.3V & 1% THD 400mW(typ.)
- ◆ Shutdown Current 0.1Ma (typ.)

Features

- ◆ Available in space-saving packages: micro SMD, MSOP, SOIC, and LLP
- ◆ Ultra low current shutdown mode
- ◆ BTL output can drive capacitive loads
- ◆ Improved pop & click circuitry eliminates noises during turn-on and turn-off transitions
- ◆ 2.2 - 5.5V operation
- ◆ No output coupling capacitors, snubber networks or bootstrap capacitors required
- ◆ Thermal shutdown protection
- ◆ Unity-gain stable
- ◆ External gain configuration capability

Applications

- Mobile Phones
- PDAs
- Portable electronic devices

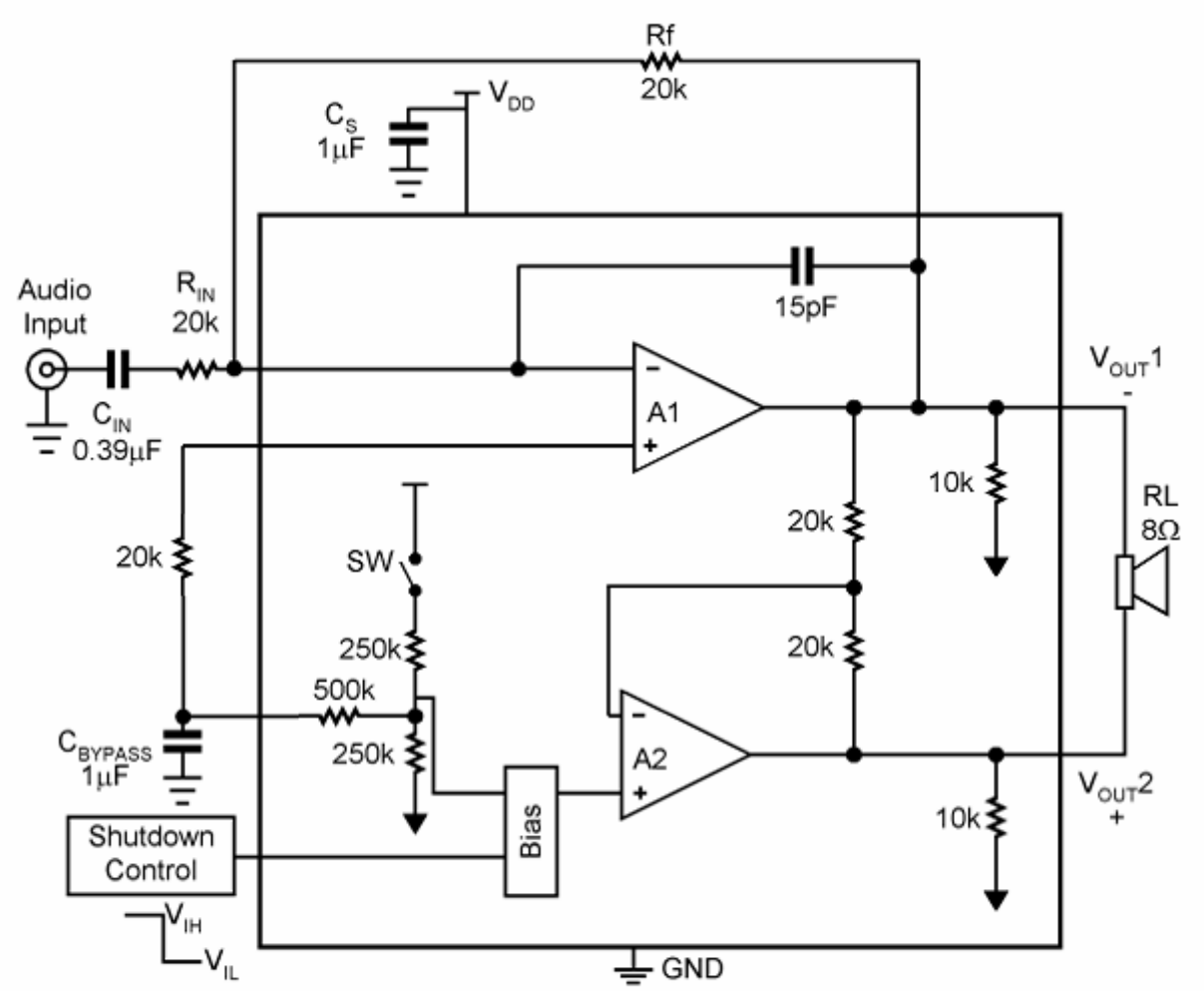


FIGURE 1. Typical Audio Amplifier Application Circuit

Absolute Maximum Ratings (Note 2)

Supply Voltage (Note 11)	6.0V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3V to VDD +0.3V
Power Dissipation (Note 3)	Internally Limited
ESD Susceptibility (Note 4)	2000V
Junction Temperature	150°C
Thermal Resistance	
θ JC (SOP)	35°C/W
θ JA (SOP)	150°C/W

θ JA (8 Bump micro SMD, Note 12) 220°C/W
θ JA (9 Bump micro SMD, Note 12) 180°C/W
θ JC (MSOP) 56°C/W
θ JA (MSOP) 190°C/W
θ JA (LLP) 220°C/W
Soldering Information
See AN-1112 "microSMD Wafers Level Chip Scale Package."
See AN-1187 "Leadless Leadframe Package (LLP)."

Operating Ratings

Temperature Range
TMIN ≤TA ≤TMAX -40°C ≤TA ≤85°C
Supply Voltage 2.2V ≤VDD ≤5.5V

Electrical Characteristics VDD = 5V (Notes 1, 2, 8)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for TA = 25°C

Symbol	Parameter	Conditions	LM4890		Units (Limits)
			Typical	Limit	
			(Note 6)	(Notes 7, 9)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A, No Load	4	8	mA (max)
		V_{IN} = 0V, I_O = 0A, 8Ω Load	5	10	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = 0V	0.1	2.0	µA (max)
V_{SDIH}	Shutdown Voltage Input High			1.2	V (min)
V_{SDIL}	Shutdown Voltage Input Low			0.4	V (max)
V_{OS}	Output Ofsett Voltage		7	50	mV (max)
$R_{OUT-GND}$	Resistor Output to GND (Note 10)		8.5	9.7	k Ω (max)
				7.0	k Ω (min)
P_O	Output Power (8 Ω)	THD = 2%(max); f = 1 kHz	1.0	0.8	W
T_{WU}	Wake-up time		170	220	ms (max)
T_{SD}	Thermal Shutdown Temperature		170	150	°C (min)
				190	°C (max)
THD+N	Total Harmonic Distortion+Noise	P_O = 0.4 Wrms; f = 1kHz	0.1		%
PSRR	Power Supply	V_{ripple} = 200mV	62 (f =	55	dB (min)

	Rejection Ratio (Note 14)	sine p-p Input Terminated with 10 ohms to ground	217Hz) 66 (f = 1kHz)		
T_{SDT}	Shut Down Time	8 Ω load	1.0		ms (max)

Electrical Characteristics VDD = 3V (Notes 1, 2, 8)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for TA = 25°C.

Symbol	**Parameter**	**Conditions**	**LM4890**		**Units (Limits)**
			Typical	**Limit**	
			(Note 6)	(Notes 7,9)	
IDD	Quiescent Power Supply Current	VIN = 0V,Io= 0A, No Load	3.5	7	mA (max)
		VIN = 0V,Io= 0A, 8 Ω Load	4.5	9	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = 0V	0.1	2.0	µA (max)
V_{SDIH}	Shutdown Voltage Input High			1.2	V (min)
V_{SDIL}	Shutdown Voltage Input Low			0.4	V (max)
V_{OS}	Output Ofsett Voltage		7	50	mV (max)
$R_{OUT-GND}$	Resistor Output to GND (Note 10)		8.5	9.7	k . (max)
				7.0	k . (min)
P_o	Output Power (8 Ω)	THD = 1%(max); f = 1 kHz	120	180	W
T_{WU}	Wake-up time		0.13	0.28	ms (max)
T_{SD}	Thermal Shutdown Temperature		170	150	°C (min)
				190	°C (max)
THD+N	Total Harmonic Distortion+Noise	P_o = 0.15 Wrms; f = 1kHz	0.1		%
PSRR	Power Supply Rejection Ratio (Note 14)	V_{ripple} = 200mV sine p-p Input Terminated with 10 ohms to ground	56 (f = 217Hz) 62 (f = 1kHz)	4.5	dB (min)

Electrical Characteristics VDD = 2.6V (Notes 1, 2, 8)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for TA = 25°C.

Symbol	Parameter	Conditions	LM4890		Units (Limits)
			Typical	Limit	
			(Note 6)	(Notes 7,9)	
IDD	Quiescent Power Supply Current	VIN = 0V,Io= 0A, No Load	2.6		mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN}$ = 0V	0.1		µA (max)
P_o	Output Power (8 Ω) Output Power (4 Ω)	THD = 1%(max); f = 1 kHz	0.2 0.22		W W
THD+N	Total Harmonic Distortion+Noise	P_o = 0.1 Wrms; f = 1kHz	0.08		%
PSRR	Power Supply Rejection Ratio (Note 14)	V_{ripple} = 200mV sine p-p Input Terminated with 10 ohms to ground	44 (f = 217Hz) 44 (f = 1kHz)		dB

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by TJMAX, JA, and the ambient temperature TA. The maximumallowable power dissipation is PDMAX = (TJMAX–TA)/ JA or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4890, see power deratingcurves for additional information.

Note 4: Human body model, 100 pF discharged through a 1.5 k . resistor.

Note 5: Machine Model, 220 pF–240 pF discharged through all pins.

Note 6: Typicals are measured at 25°C and represent the parametric norm.

Note 7: Limits are guaranteed to ASIC's AOQL (Average Outgoing Quality Level).

Note 8: For micro SMD only, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase ISD by a maximum of µA.

Note 9: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note 10: ROUT is measured from each of the output pins to ground. This value represents the parallel

combination of the 10k ohm output resistors and the two 20kohm resistors.

Note 11: If the product is in shutdown mode and VDD exceeds 6V (to a max of 8V VDD), then most of the excess current will flow through the ESD protection circuits.

If the source impedance limits the current to a max of 10 ma, then the part will be protected. If the part is enabled when VDD is greater than 5.5V and less than 6.5V, no damage will occur, although operational life will be reduced. Operation above 6.5V with no current limit will result in permanent damage.

Note 12: All bumps have the same thermal resistance and contribute equally when used to lower thermal resistance. All bumps must be connected to achieve specified thermal resistance.

Note 13: Maximum power dissipation (PDMAX) in the device occurs at an output power level significantly below full output power. PDMAX can be calculated using Equation 1 shown in the Application section. It may also be obtained from the power dissipation graphs.

Note 14: PSRR is a function of system gain. Specifications apply to the circuit in Figure 1 where AV = 2. Higher system gains will reduce PSRR value by the amount of gain increase. A system gain of 10 represents a gain increase of 14dB. PSRR will be reduced by 14dB and applies to all operating voltages.

External Components Description (*Figure 1*)

Components		Functional Description
1.	R_{IN}	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high pass filter with C_{IN} at $f_C = 1/(2 \cdot R_{IN}C_{IN})$.
2.	C_{IN}	Input coupling capacitor which blocks the DC voltage at the amplifier's input terminals. Also creates a highpass filter with R_{IN} at $f_c = 1/(2 \cdot R_{IN}C_{IN})$. Refer to the section, **Proper Selection of External Components**, for an explanation of how to determine the value of C_{IN}.
3.	R_f	Feedback resistance which sets the closed-loop gain in conjunction with R_{IN}.
4.	C_S	Supply bypass capacitor which provides power supply filtering. Refer to the section, **Power Supply Bypassing**, for information concerning proper placement and selection of the supply bypass capacitor, C_{BYPASS}.
5.	C_{BYPASS}	Bypass pin capacitor which provides half-supply filtering. Refer to the section, **Proper Selection of External Components**, for information concerning proper placement and selection of C_{BYPASS}.

Application Information

BRIDGED CONFIGURATION EXPLANATION

As shown in *Figure 1*, the LM4890 has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity- gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_{IN} while the second amplifier's gain is fixed by the two internal 20k $\cdot$ resistors. *Figure 1* shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but

out of phase by 180°. Consequently, the differential gain for the IC is

$A_{VD} = 2 * (R_f / R_{IN})$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as “bridged mode” is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier’s closed-loop gain without causing excessive clipping, please refer to the **Audio Power Amplifier Design** section.

A bridge configuration, such as the one used in the LM4890, also creates a second advantage over single-ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the LM4890 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 1.

$$P_{DMAX} = 4*(V_{DD})\ 2/\ (2\quad 2R_L)\ (1)$$

It is critical that the maximum junction temperature T_{JMAX} of 150°C is not exceeded. TJMAX can be determined from the power derating curves by using PDMAX and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced, resulting in higher PDMAX. Additional copper foil can be added to any of the leads connected to the LM4890. Refer to the **APPLICATION INFORMATION** on the LM4890 reference design board for an example of good heat sinking. If TJMAX still exceeds 150°C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power. Refer to the **Typical Performance Characteristics** curves for power dissipation information for different output powers and output loading.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10 µF

tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the LM4890. The selection of a bypass capacitor, especially CBYPASS, is dependent upon PSRR requirements, click and pop performance (as explained in the section, **Proper Selection of External Components**), system cost, and size constraints.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4890 contains a shutdown pin to externally turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the shutdown pin.

By switching the shutdown pin to ground, the LM4890 supply current draw will be minimized in idle mode. While the device will be disabled with shutdown pin voltages less than 0.5VDC, the idle current may be greater than the typical value of 0.1μA. (Idle current is measured with the shutdown pin grounded).

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry to provide a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch in conjunction with an external pull-up resistor. When the switch is closed, the shutdown pin is connected to ground and disables the amplifier.

If the switch is open, then the external pull-up resistor will enable the LM4890. This scheme uarantees that the shutdown pin will not float thus preventing unwanted state changes.

SHUTDOWN OUTPUT IMPEDANCE

For Rf = 20k ohms:

Z_{OUT1} (between Out1 and GND) = 10k||50k||R_f = 6k

Z_{OUT2} (between Out2 and GND) = 10k||(40k+(10k||R_f)) = 8.3k

Z_{OUT1-2} (between Out1 and Out2) = 40k||(10k+(10k||R_f)) = 11.7k

The -3dB roll off for these measurements is 600kHz

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the LM4890 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The LM4890 is unity-gain stable which gives the designer maximum system flexibility. The LM4890 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1Vrms are available from sources such as audio codecs. Please refer to the section, **Audio Power Amplifier Design**, for a more complete explanation of proper gain selection.

Besides gain, one of the major considerations is the closedloop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in *Figure 1*.

The input coupling capacitor, CIN, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

Selection Of Input Capacitor Size

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, CIN. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 VDD). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, CBYPASS, is the most critical component to minimize turn-on pops since it determines how fast the LM4890 turns on. The slower the LM4890's outputs ramp to their quiescent DC voltage (nominally 1/2VDD), the smaller the turn-on pop. Choosing CBYPASS equal to 1.0µF along with a small value of CIN, (in the range of 0.1µF to 0.39µF), should produce a virtually clickless and popless shutdown function. While the device will function properly, (no oscillations or motorboating), with CBYPASS equal to 0.1µF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of CBYPASS equal to 1.0µF is recommended in all but the most cost sensitive designs.

AUDIO POWER AMPLIFIER DESIGN

A 1W/8Ω AUDIO AMPLIFIER

Given:

Power Output	1 Wrms
Load Impedance	8Ω
Input Level	1 Vrms
Input Impedance	20 kΩ
Bandwidth	100 Hz–20 kHz ± 0.25 dB

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the **Typical Performance Characteristics** section, the supply rail can be easily found. A second way to determine the minimum supply rail is to calculate the required Vopeak using Equation 2 and add the output voltage. Using this method, the minimum supply voltage would be (Vopeak + (V_{ODTOP} + V_{ODBOT})), where V_{ODBOT} and V_{ODTOP} are extrapolated from the Dropout Voltage vs Supply Voltage curve in the **Typical Performance Characteristics** section.

$$V_{OPEAK} = \sqrt{(2R_LP_O)}$$

5V is a standard voltage which in most applications is chosen for the supply rail. Extra supply voltage creates headroom that allows the LM4890 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section. Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 3.

$A_{VD} \geq \surd (P_O R_L) / (V_{IN}) = V_{orms} / V_{inrms}$ (3)

$R_f / R_{IN} = A_{VD} / 2$

From Equation 3, the minimum A_{VD} is 2.83; use A_{VD} = 3.

Since the desired input impedance is 20 kΩ, and with an A_{VD} gain of 3, a ratio of 1.5:1 of R_f to R_{IN} results in an allocation of R_{IN} = 20 kΩ and Rf = 30 kΩ. The final design step is to address the bandwidth requirements which must be stated as a pair of −3 dB frequency points. Five times away from a −3 dB point is 0.17 dB down from passband response which is better than the required ±0.25 dB specified.

f_L = 100Hz/5 = 20Hz

f_H = 20kHz * 5 = 100kHz

As stated in the **External Components** section, R_{IN} in conjunction with C_{IN} create a highpass filter.

$C_{IN} \geq 1/(2\pi * 20\ k\Omega * 20Hz) = 0.397\mu F$; use 0.39μF

The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, A_{VD}. With a A_{VD} = 3 and f_H = 100kHz, the resulting GBWP = 300kHz which is much smaller than the LM4890 GBWP of 2.5MHz. This calculation shows that if a designer has a need to design an amplifier with a higher differential gain, the LM4890 can still be used without running into bandwidth limitations. The

LM4890 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. However, if a closed-loop differential gain of greater than 10 is required, a feedback capacitor (C4) may be needed as shown in **Figure 2** to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates possible high frequency oscillations. Care should be taken when calculating the -3dB frequency in that an incorrect combination of R_3 and C_4 will cause rolloff before 20kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is R_3 = 20kΩ and C_4 = 25pf. These components result in a -3dB point of approximately 320 kHz.

Application Information (Continued)

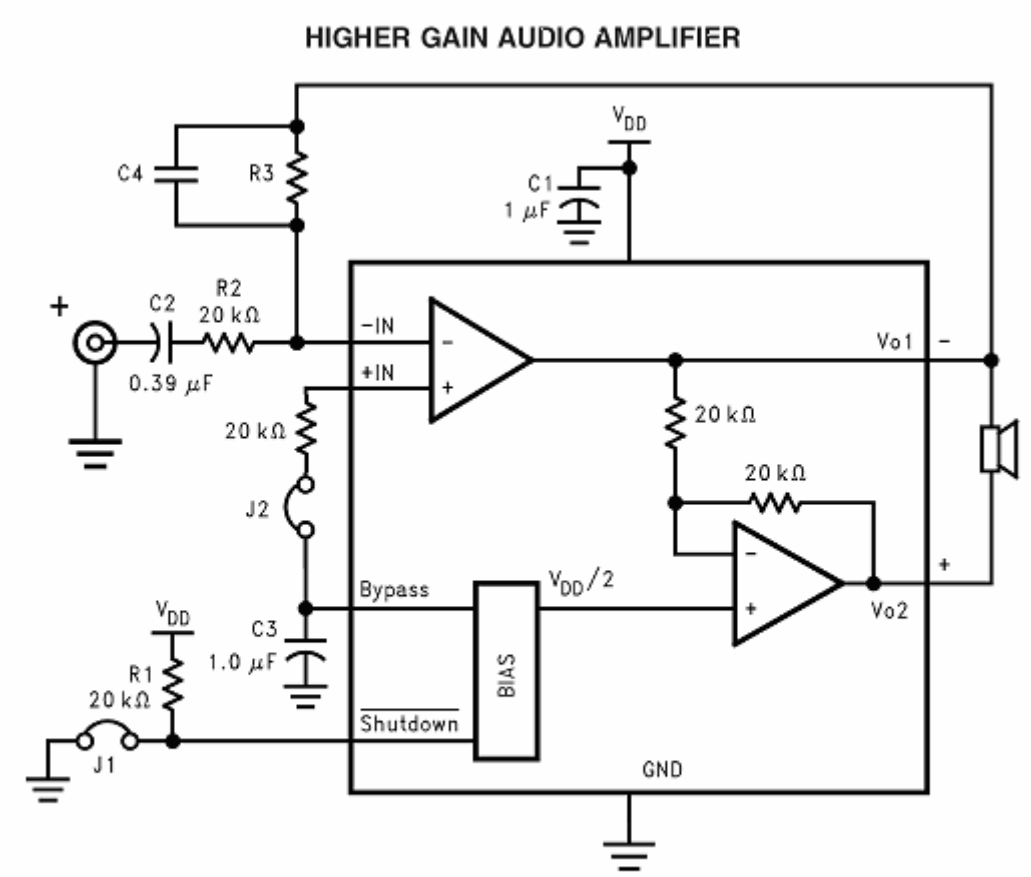


FIGURE 2.

DIFFERENTIAL AMPLIFIER CONFIGURATION FOR LM4890

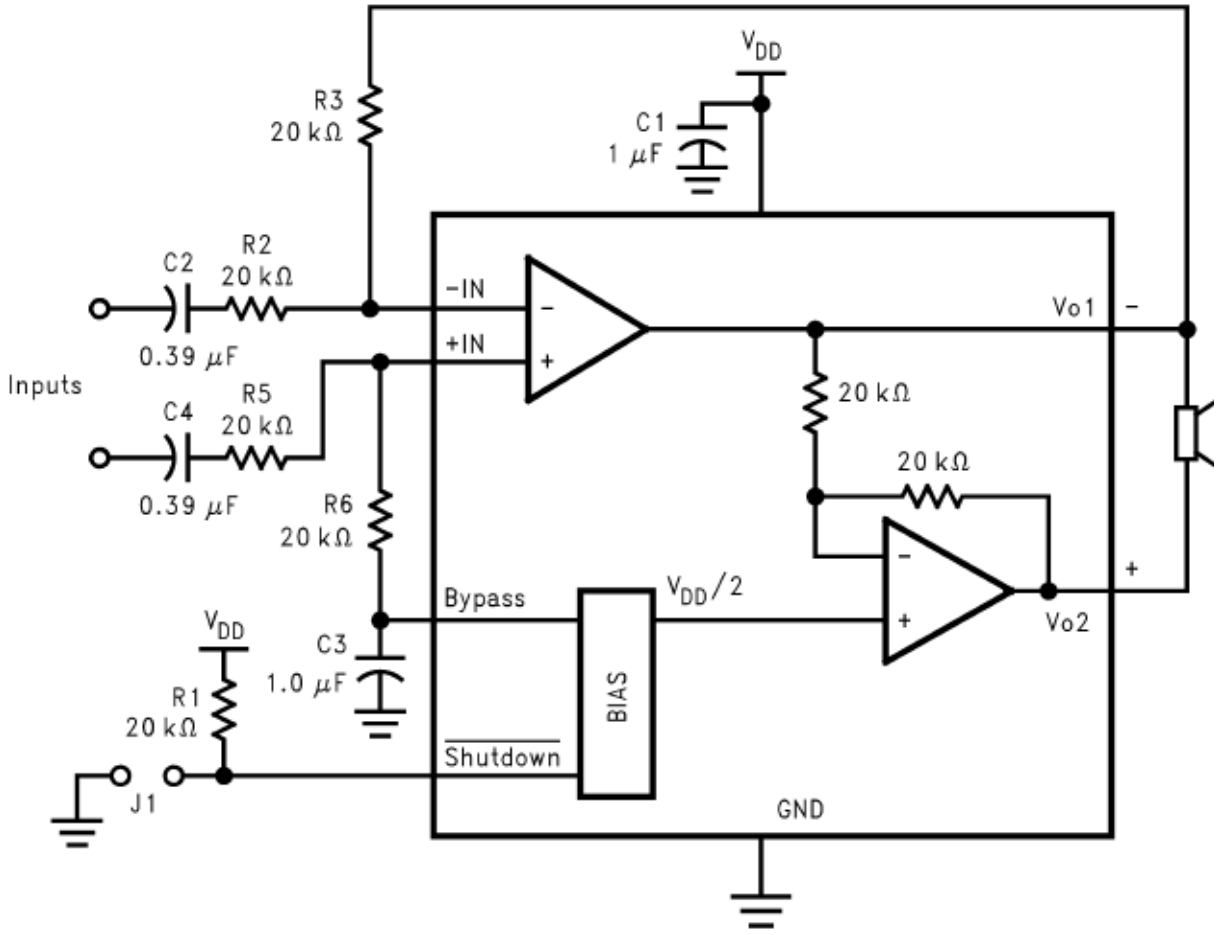


FIGURE 3
REFERENCE DESIGN BOARD and LAYOUT - micro SMD

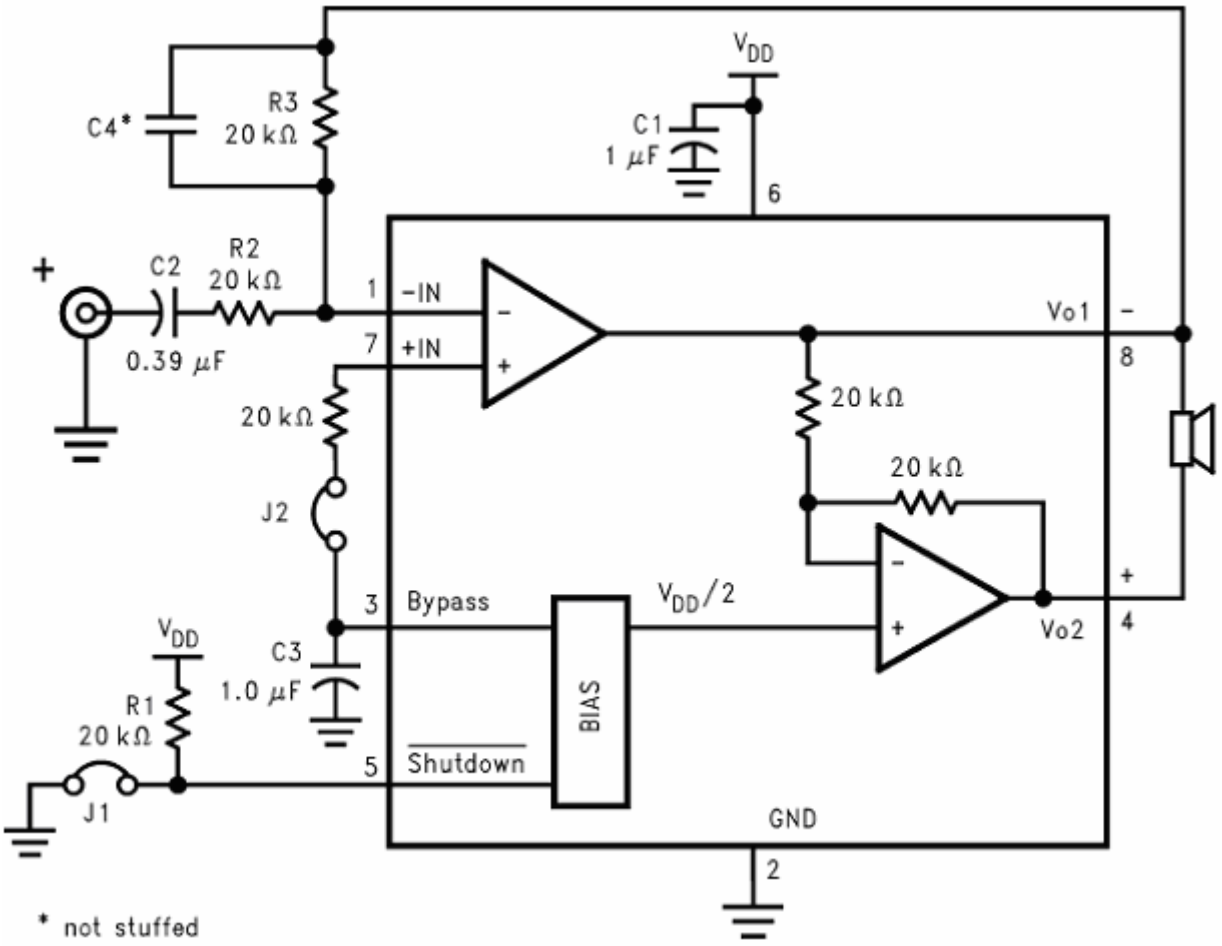
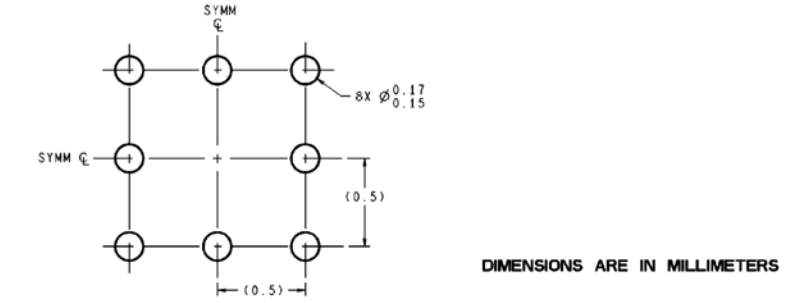

C4*
R3
20 kΩ
VDD
C1
1 µF
6
+
C2
0.39 µF
R2
20 kΩ
1
-IN
7
+IN
Vo1
8
20 kΩ
20 kΩ
J2
3
Bypass
VDD/2
Vo2
4
VDD
C3
1.0 µF
R1
20 kΩ
BIAS
5
Shutdown
J1
GND
2
* not stuffed

FIGURE 4.

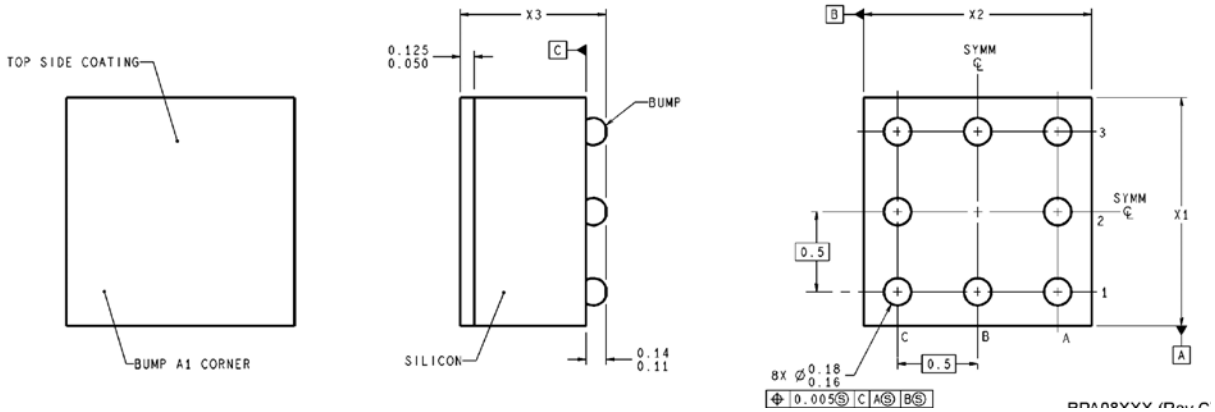
Physical Dimensions inches (millimeters)

unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

LAND PATTERN RECOMMENDATION



Note: Unless otherwise specified.

1. Epoxy coating.
2. 63Sn/37Pb eutectic bump.
3. Recommend non-solder mask defined landing pad.
4. Pin 1 is established by lower left corner with respect to text orientation pins are numbered counterclockwise.
5. Reference JEDEC registration MO-211, variation BC.

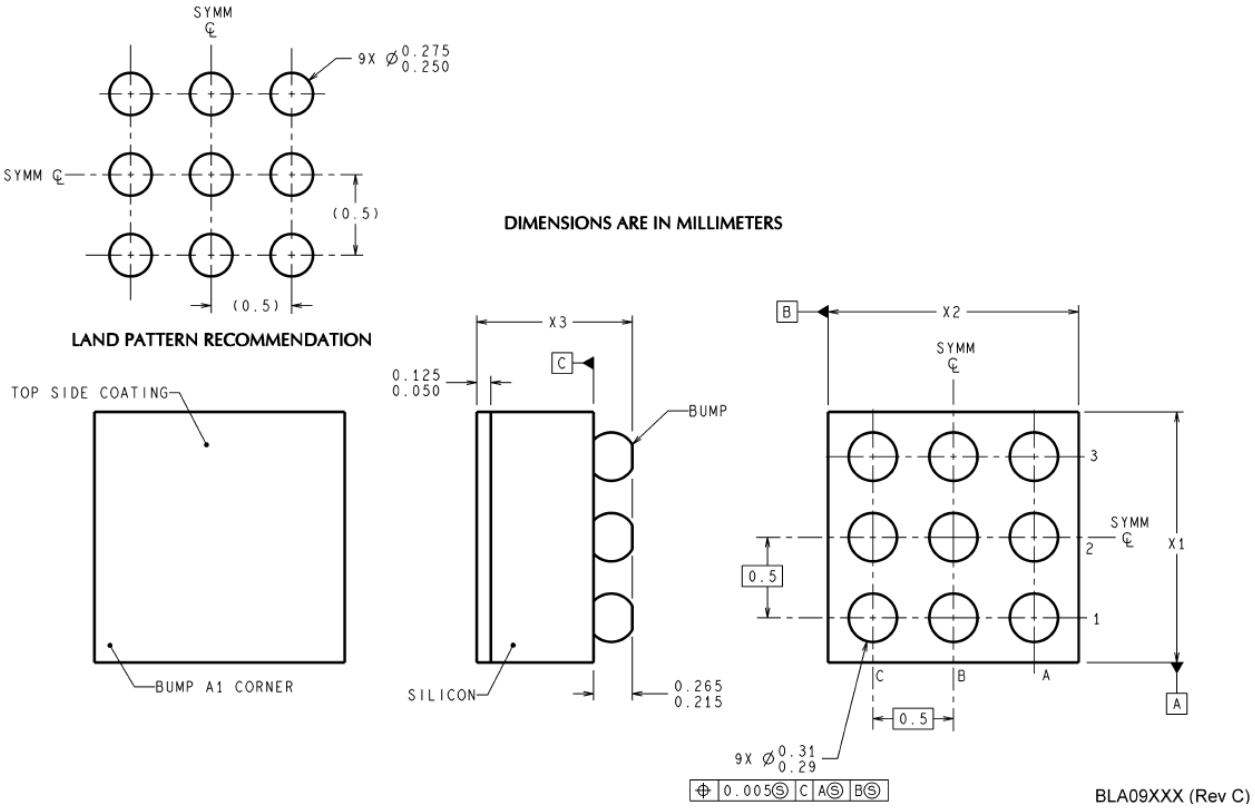
8-Bump micro SMD

Order Number LM4890IBP, LM4890IBPX

NS Package Number BPA08DDB

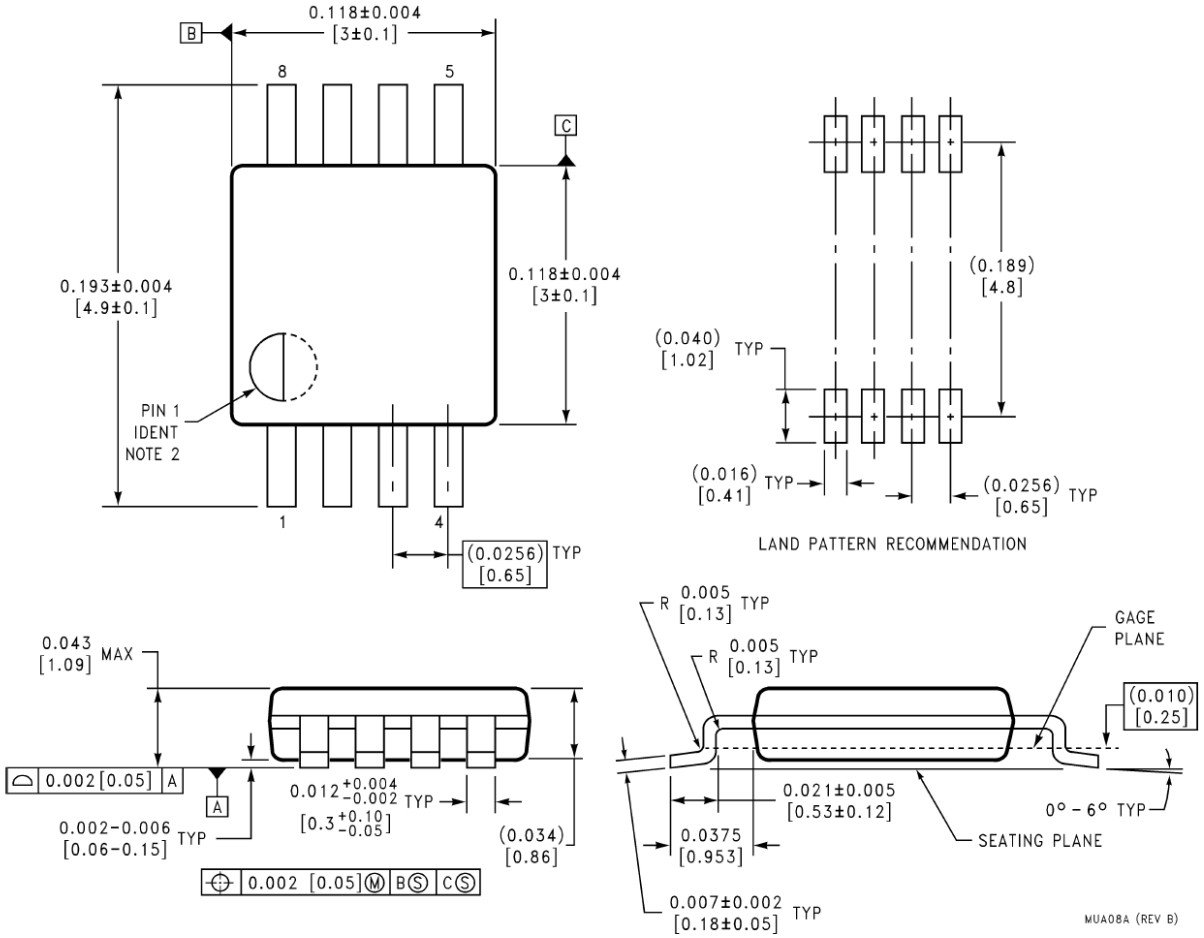
X1 = 1.361±0.03 X2 = 1.361±0.03 X3 = 0.850±0.10

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



9-Bump micro SMD
Order Number LM4890IBL, LM4890IBLX
NS Package Number BLA09AAB
X1 = 1.514±0.03 X2 = 1.514±0.03 X3 = 0.945±0.10

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

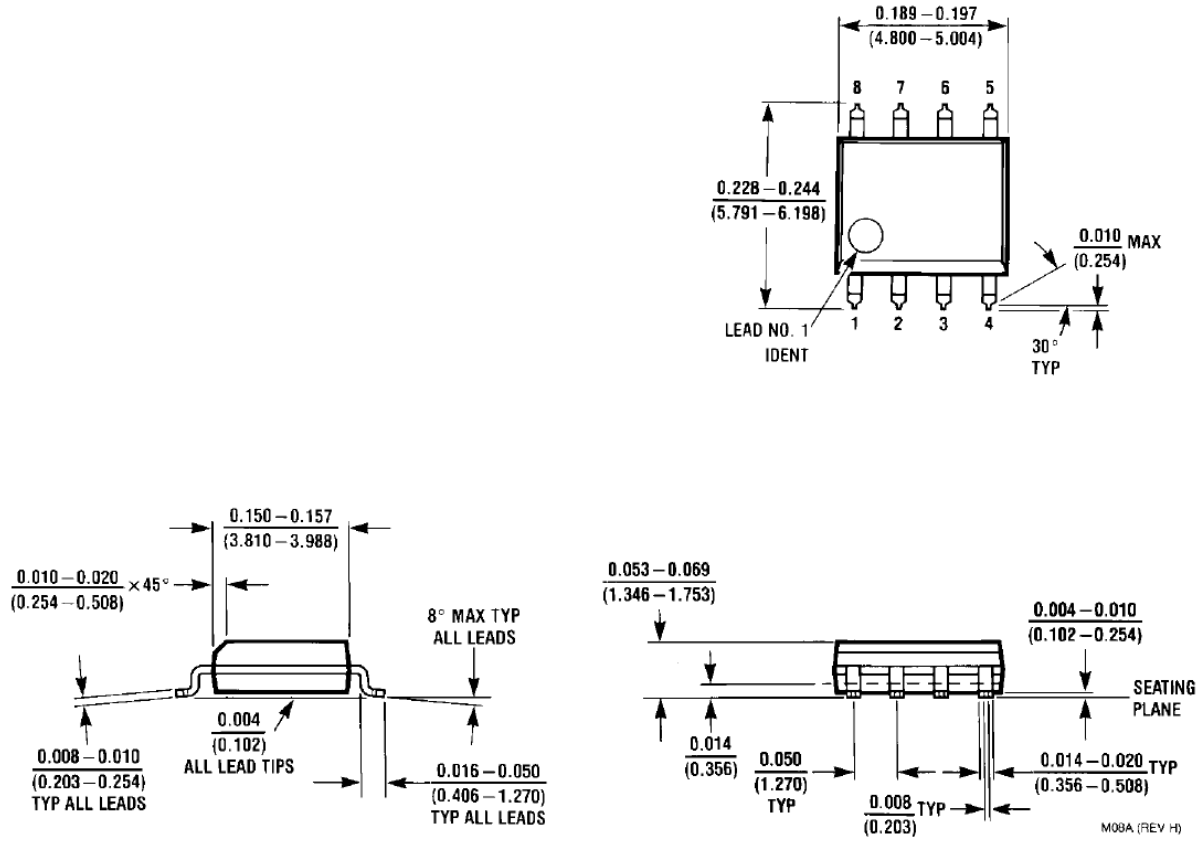


MSOP

Order Number LM4890MM

NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



SO

Order Number LM4890M

NS Package Number M08A

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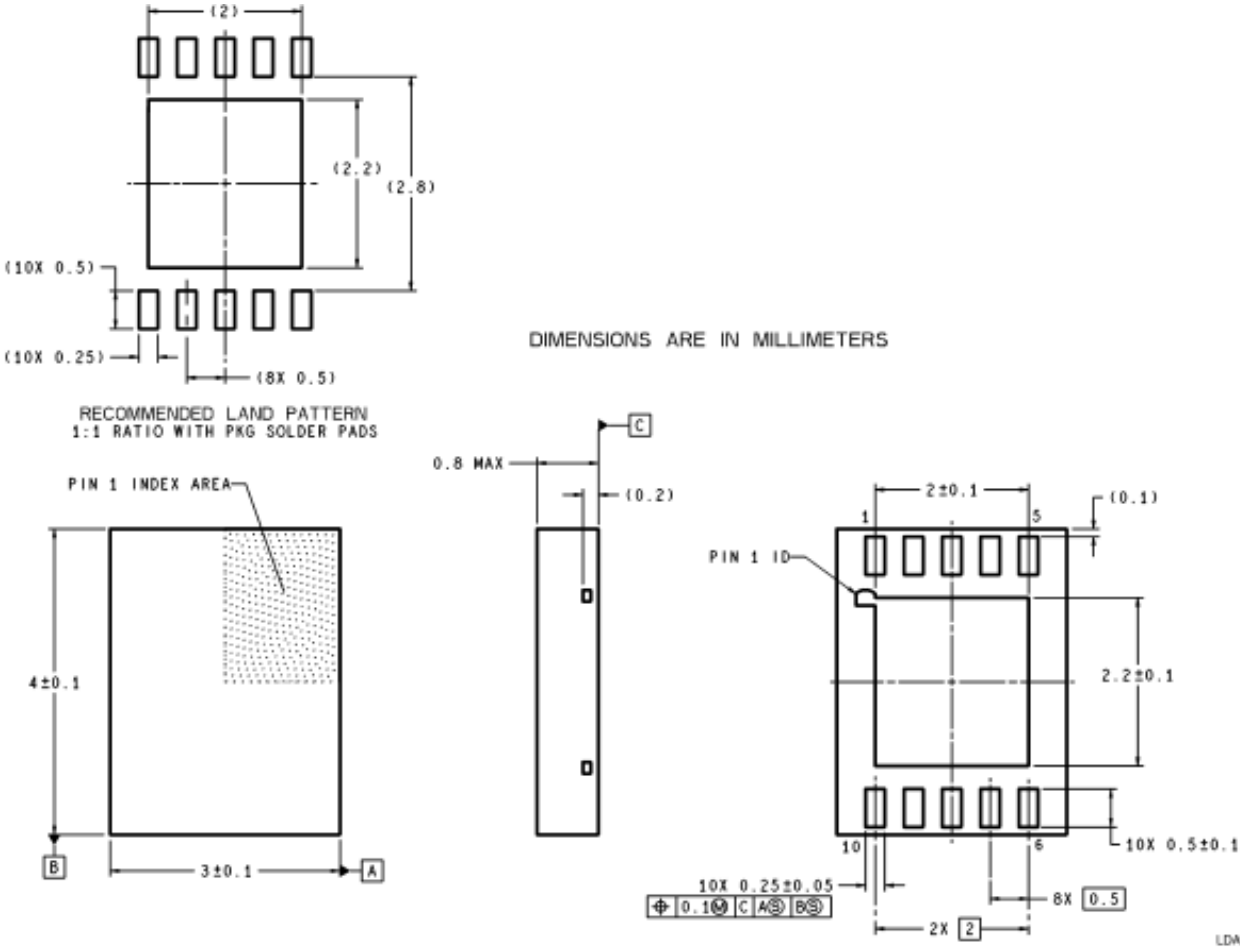
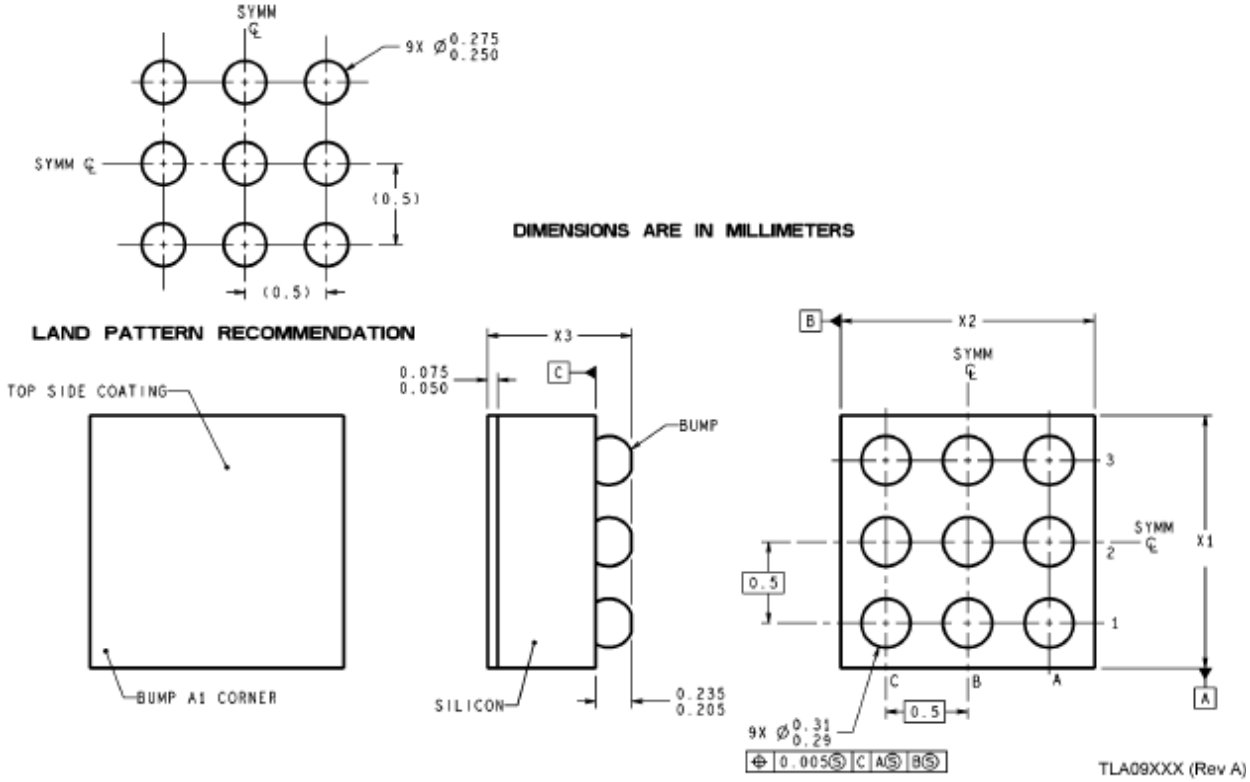


LLP
Order Number LM4890LD
NS Package Number LDA10B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



9-Bump micro SMD
Order Number LM4890ITL, LM4890ITLX
NS Package Number TLA09AAA
X1 = 1.514±0.03 X2 = 1.514±0.03 X3 = 0.600±0.075

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. The TIGER ELELTRONIC CO., recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.