TIGER ELECTRONIC CO.,LTD

DS1302

Trickle Charge Timekeeping Chip

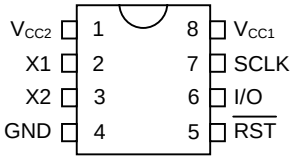
FEATURES

- Real time clock counts seconds, minutes hours, date of the month, month, day of the week, and year with leap year compensation valid up to 2100
- 31 x 8 RAM for scratchpad data storage
- Serial I/O for minimum pin count
- 2.0–5.5V full operation
- Uses less than 300 nA at 2.0V
- Single–byte or multiple–byte (burst mode) data transfer for read or write of clock or RAM data
- 8–pin DIP or optional 8–pin SOICs for surface mount
- Simple 3–wire interface
- TTL–compatible (V_{CC} = 5V)
- Optional industrial temperature range –40°C to +85°C
- DS1202 compatible
- Recognized by Underwriters Laboratory

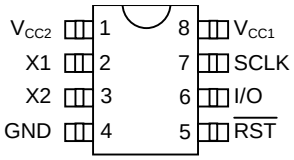
ORDERING INFORMATION

PART #	DESCRIPTION
DS1302	8–Pin DIP
DS1302N	8-Pin DIP (Industrial)
DS1302S	8–Pin SOIC (200 mil)
DS1302SN	8–Pin SOIC (Industrial)
DS1302Z	8–Pin SOIC (150 mil)
DS1302ZN	8–Pin SOIC (Industrial)
DS1302S-16	16-Pin SOIC (300 mil)
DS1302SN-16	16-Pin SOIC (Industrial)

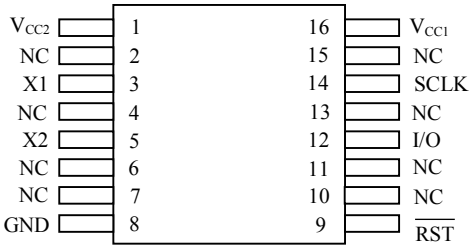
PIN ASSIGNMENT



DS1302
8-Pin DIP (300 mil)



DS1302S 8-Pin SOIC (200 mil)
DS1302Z 8-Pin SOIC (150 mil)



16-Pin SOIC

PIN DESCRIPTION

X1, X2	– 32.768 kHz Crystal Pins
GND	– Ground
$\overline{RST}$	– Reset
I/O	– Data Input/Output
SCLK	– Serial Clock
V_{CC1}, V_{CC2}	– Power Supply Pins

DESCRIPTION

The DS1302 Trickle Charge Timekeeping Chip contains a real time clock/calendar and 31 bytes of static RAM. It communicates with a microprocessor via a simple serial interface. The real time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24–hour or 12–hour format with an AM/PM indicator

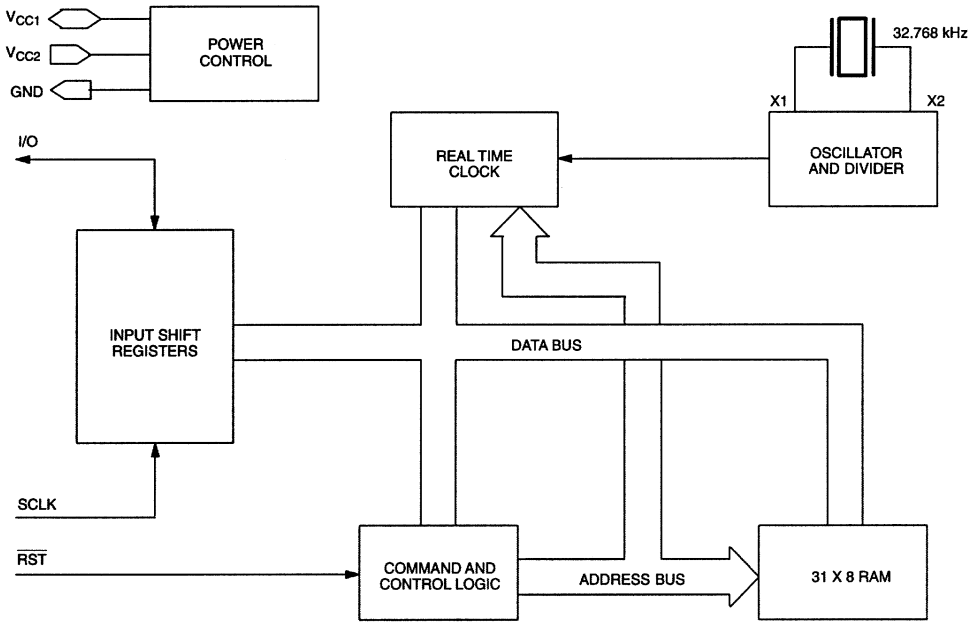
Interfacing the DS1302 with a microprocessor is simplified by using synchronous serial communication. Only three wires are required to communicate with the clock/RAM: (1) $\overline{RST}$ (Reset), (2) I/O (Data line), and (3) SCLK (Serial clock). Data can be transferred to and from the clock/RAM 1 byte at a time or in a burst of up to 31 bytes. The DS1302 is designed to operate on very low power and retain data and clock information on less than 1 microwatt.

The DS1302 is the successor to the DS1202. In addition to the basic timekeeping functions of the DS1202, the DS1302 has the additional features of dual power pins for primary and back–up power supplies, programmable trickle charger for V_{CC1}, and seven additional bytes of scratchpad memory.

OPERATION

The main elements of the Serial Timekeeper are shown in Figure 1: shift register, control logic, oscillator, real time clock, and RAM.

DS1302 BLOCK DIAGRAM Figure 1



SIGNAL DESCRIPTIONS

V_{CC1} – V_{CC1} provides low power operation in single supply and battery operated systems as well as low power battery backup. In systems using the trickle charger, the rechargeable energy source is connected to this pin.

V_{CC2} – Vcc2 is the primary power supply pin in a dual supply configuration. V_{CC1} is connected to a backup source to maintain the time and date in the absence of primary power.

The DS1302 will operate from the larger of V_{CC1} or V_{CC2}. When V_{CC2} is greater than V_{CC1} + 0.2V, V_{CC2} will power the DS1302. When V_{CC2} is less than V_{CC1}, V_{CC1} will power the DS1302.

SCLK (Serial Clock Input) – SCLK is used to synchronize data movement on the serial interface.

I/O (Data Input/Output) – The I/O pin is the bi-directional data pin for the 3-wire interface.

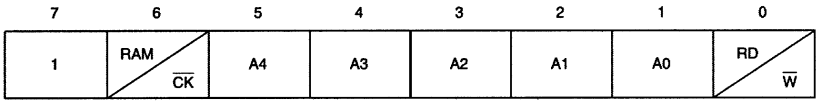
$\overline{RST}$ (Reset) – The reset signal must be asserted high during a read or a write.

X1, X2 – Connections for a standard 32.768 kHz quartz crystal. The internal oscillator is designed for operation with a crystal having a specified load capacitance of 6 pF. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, "Crystal Considerations with Real Time Clocks." The DS1302 can also be driven by an external 32.768 kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

COMMAND BYTE

The command byte is shown in Figure 2. Each data transfer is initiated by a command byte. The MSB (Bit 7) must be a logic 1. If it is 0, writes to the DS1302 will be disabled. Bit 6 specifies clock/calendar data if logic 0 or RAM data if logic 1. Bits 1 through 5 specify the designated registers to be input or output, and the LSB (bit 0) specifies a write operation (input) if logic 0 or read operation (output) if logic 1. The command byte is always input starting with the LSB (bit 0).

ADDRESS/COMMAND BYTE Figure 2



RESET AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input serves two functions. First, $\overline{RST}$ turns on the control logic which allows access to the shift register for the address/command sequence. Second, the $\overline{RST}$ signal provides a method of terminating either single byte or multiple byte data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock. If the $\overline{RST}$ input is low all data transfer terminates and the I/O pin goes to a high impedance state. Data transfer is illustrated in Figure 3. At power–up, $\overline{RST}$ must be a logic 0 until V_{CC} > 2.0 volts. Also SCLK must be at a logic 0 when $\overline{RST}$ is driven to a logic 1 state.

DATA INPUT

Following the eight SCLK cycles that input a write command byte, a data byte is input on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored should they inadvertently occur. Data is input starting with bit 0.

DATA OUTPUT

Following the eight SCLK cycles that input a read command byte, a data byte is output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles retransmit the data bytes should they inadvertently occur so long as $\overline{RST}$ remains high. This operation permits continuous burst mode read capability. Also, the I/O pin is tri–stated upon each rising edge of SCLK. Data is output starting with bit 0.

BURST MODE

Burst mode may be specified for either the clock/calendar or the RAM registers by addressing location 31 decimal (address/command bits 1 through 5 = logic 1). As before, bit 6 specifies clock or RAM and bit 0

specifies read or write. There is no data storage capacity at locations 9 through 31 in the Clock/Calendar Registers or location 31 in the RAM registers. Reads or writes in burst mode start with bit 0 of address 0.

When writing to the clock registers in the burst mode, the first eight registers must be written in order for the data to be transferred. However, when writing to RAM in burst mode it is not necessary to write all 31 bytes for the data to transfer. Each byte that is written to will be transferred to RAM regardless of whether all 31 bytes are written or not.

CLOCK/CALENDAR

The clock/calendar is contained in seven write/read registers as shown in Figure 4. Data contained in the clock/ calendar registers is in binary coded decimal format (BCD).

CLOCK HALT FLAG

Bit 7 of the seconds register is defined as the clock halt flag. When this bit is set to logic 1, the clock oscillator is stopped and the DS1302 is placed into a low–power standby mode with a current drain of less than 100 nanoamps. When this bit is written to logic 0, the clock will start. The initial power on state is not defined.

AM-PM/12-24 MODE

Bit 7 of the hours register is defined as the 12– or 24–hour mode select bit. When high, the 12–hour mode is selected. In the 12–hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24–hour mode, bit 5 is the second 10-hour bit (20 – 23 hours).

WRITE PROTECT BIT

Bit 7 of the control register is the write-protect bit. The first seven bits (bits 0 – 6) are forced to 0 and will always read a 0 when read. Before any write operation to the clock or RAM, bit 7 must be 0. When high, the write protect bit prevents a write operation to any other register. The initial power on state is not defined. Therefore the WP bit should be cleared before attempting to write to the device.

TRICKLE CHARGE REGISTER

This register controls the trickle charge characteristics of the DS1302. The simplified schematic of Figure 5 shows the basic components of the trickle charger. The trickle charge select (TCS) bits (bits 4 -7) control the selection of the trickle charger. In order to prevent accidental enabling, only a pattern of 1010 will enable the trickle charger. All other patterns will disable the trickle charger. The DS1302 powers up with the trickle charger disabled. The diode select (DS) bits (bits 2 – 3) select whether one diode or two diodes are connected between V_{CC2} and V_{CC1}. If DS is 01, one diode is selected or if DS is 10, two diodes are selected. If DS is 00 or 11, the trickle charger is disabled independently of TCS. The RS bits (bits 0 -1) select the resistor that is connected between V_{CC2} and V_{CC1}. The resistor selected by the resistor select (RS) bits is as follows:

RS Bits	Resistor	Typical Value
00	None	None
01	R1	2 kΩ
10	R2	4 kΩ
11	R3	8 kΩ

If RS is 00, the trickle charger is disabled independently of TCS.

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 5 volt is applied to V_{CC2} and a super cap is connected to V_{CC1}. Also assume that the trickle charger has been enabled with one diode and resistor R1 between V_{CC2} and V_{CC1}. The maximum current I_{max} would therefore be calculated as follows:

$$I_{max} = (5.0V - \text{diode drop}) / R1$$
$$\sim (5.0V - 0.7V) / 2\ k\Omega$$
$$\sim 2.2\ mA$$

Obviously, as the super cap charges, the voltage drop between V_{CC2} and V_{CC1} will decrease and therefore the charge current will decrease.

CLOCK/CALENDAR BURST MODE

The clock/calendar command byte specifies burst mode operation. In this mode the first eight clock/calendar registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

If the write protect bit is set high when a write clock/calendar burst mode is specified, no data transfer will occur to any of the eight clock/calendar registers (this includes the control register). The trickle charger is not accessible in burst mode.

At the beginning of a clock burst read, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

RAM

The static RAM is 31 x 8 bytes addressed consecutively in the RAM address space.

RAM BURST MODE

The RAM command byte specifies burst mode operation. In this mode, the 31 RAM registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

REGISTER SUMMARY

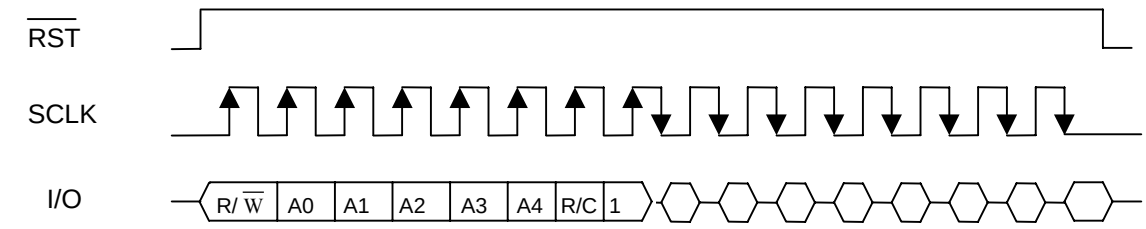
A register data format summary is shown in Figure 4.

CRYSTAL SELECTION

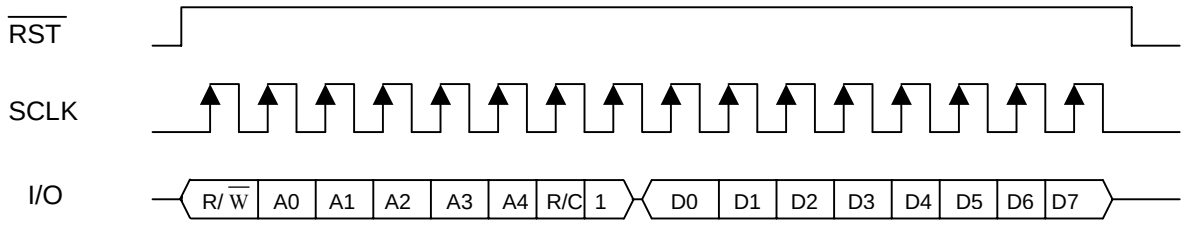
A 32.768 kHz crystal can be directly connected to the DS1302 via X1 and X2. The crystal selected for use should have a specified load capacitance (CL) of 6 pF. For more information on crystal selection and crystal layout consideration, please consult Application Note 58, “Crystal Considerations with Real Time Clocks."

DATA TRANSFER SUMMARY Figure 3

SINGLE BYTE READ

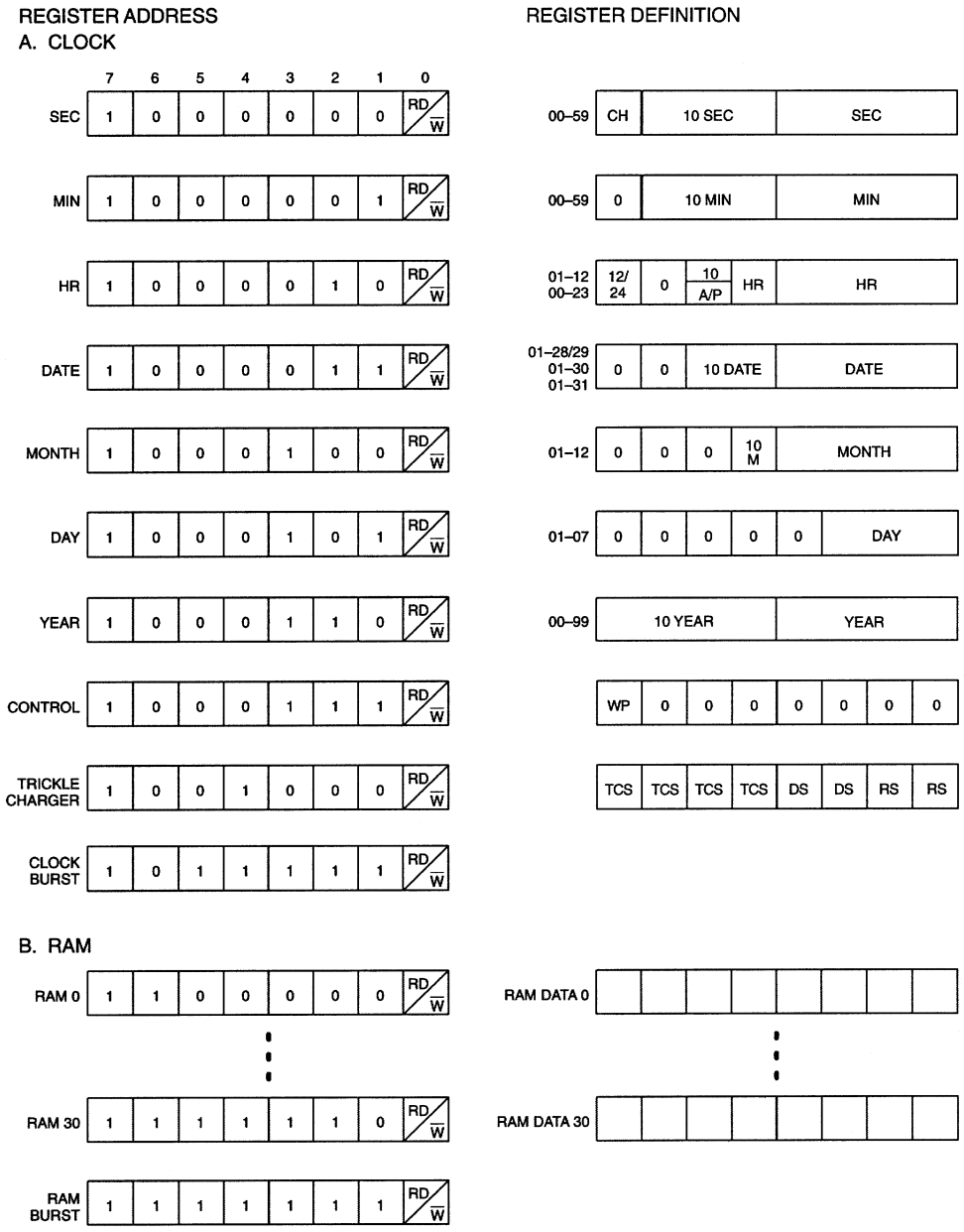


SINGLE BYTE WRITE

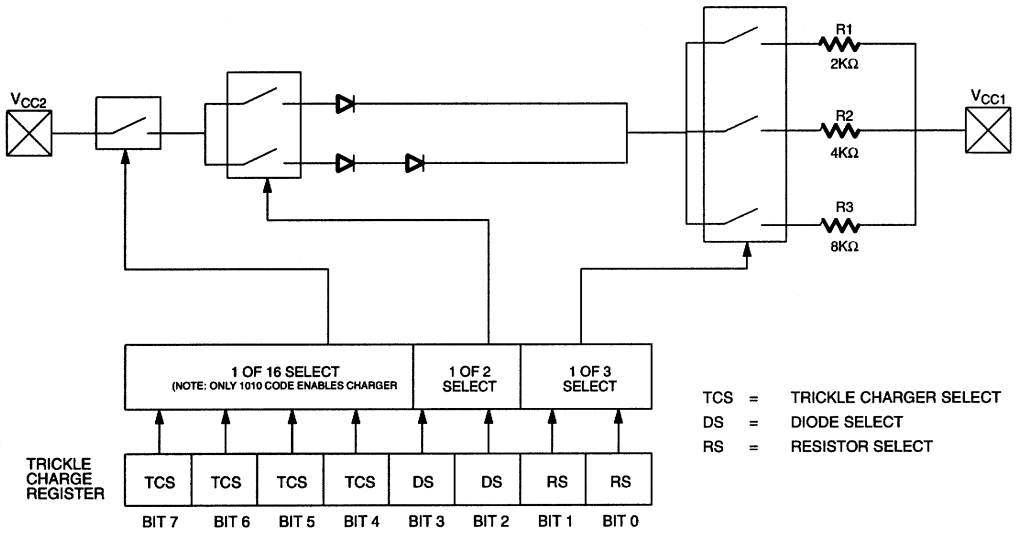


In burst mode, $\overline{RST}$ is kept high and additional SCLK cycles are sent until the end of the burst.

REGISTER ADDRESS/DEFINITION Figure 4



DS1302 PROGRAMMABLE TRICKLE CHARGER Figure 5



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to 70°C or - 40°C to +85°C for industrial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds (DIP) See IPC/JEDEC Standard J-STD-020A for Surface Mount Devices

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0ºC to 70ºC or -40°C to +85°C)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Supply Voltage V_{CC1}, V_{CC2}	V_{CC1}, V_{CC2}		2.0		5.5	V	1, 11
Logic 1 Input	V_{IH}		2.0		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	V_{CC}=2.0V	-0.3		+0.3	V	1
		V_{CC}=5V	–0.3		+0.8		

*-40°C to +85°C for industrial device.

DC ELECTRICAL CHARACTERISTICS

(0ºC to 70ºC or -40°C to +85°C; V_{CC} = 2.0 to 5.5V*)

PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}				+500	µA	6
I/O Leakage	I_{LO}				+500	µA	6
Logic 1 Output	V_{OH}	V_{CC}=2.0V	1.6			V	2
		V_{CC}=5V	2.4				
Logic 0 Output	V_{OL}	V_{CC}=2.0V			0.4	V	3
		V_{CC}=5V			0.4		
Active Supply Current	I_{CC1A}	V_{CC1}=2.0V			0.4	mA	5, 12
		V_{CC1}=5V			1.2		
Timekeeping Current	I_{CC1T}	V_{CC1}=2.0V			0.3	µA	4, 12
		V_{CC1}=5V			1		
Standby Current	I_{CC1S}	V_{CC1}=2.0V			100	nA	10, 12, 14
		V_{CC1}=5V			100		
		IND			200		
Active Supply Current	I_{CC2A}	V_{CC2}=2.0V			0.425	mA	5, 13
		V_{CC2}=5V			1.28		
Timekeeping Current	I_{CC2T}	V_{CC2}=2.0V			25.3	µA	4, 13
		V_{CC2}=5V			81		
Standby Current	I_{CC2S}	V_{CC2}=2.0V			25	µA	10, 13
		V_{CC2}=5V			80		
Trickle Charge Resistors	R1 R2 R3			2 4 8		kΩ kΩ kΩ	
Trickle Charge Diode Voltage Drop	V_{TD}			0.7		V	

*Unless otherwise noted.

CAPACITANCE

(t_A = 25ºC)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		10		pF	
I/O Capacitance	$C_{I/O}$		15		pF	
Crystal Capacitance	C_X		6		pF	

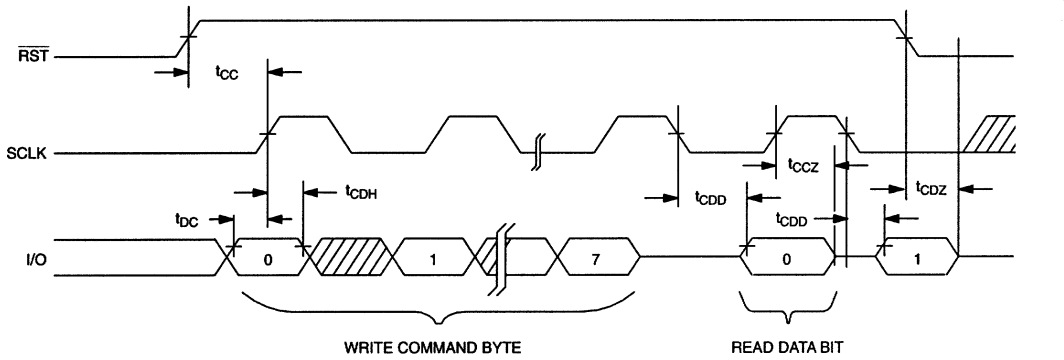
AC ELECTRICAL CHARACTERISTICS

(0ºC to 70ºC or -40°C to +85°C; V_{CC} = 2.0 to 5.5V*)

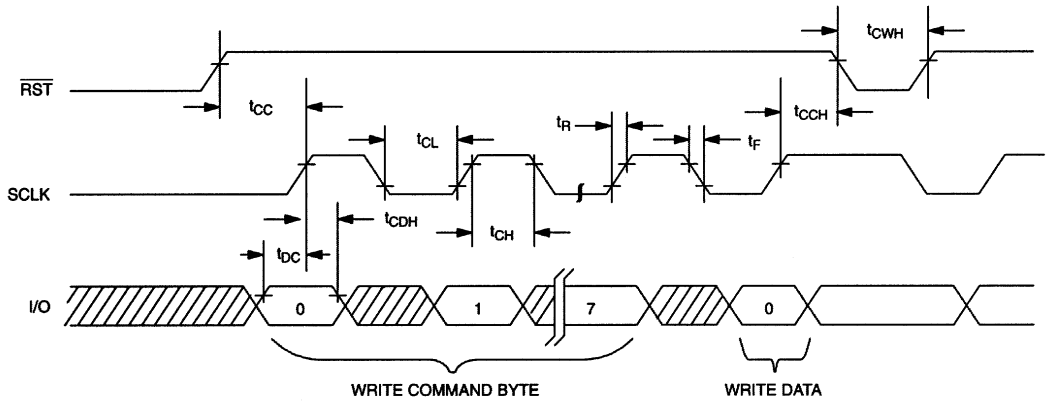
PARAMETER	SYMBOL		MIN	TYP	MAX	UNITS	NOTES
Data to CLK Setup	t_{DC}	V_{CC}=2.0V	200			ns	7
		V_{CC}=5V	50				
CLK to Data Hold	t_{CDH}	V_{CC}=2.0V	280			ns	7
		V_{CC}=5V	70				
CLK to Data Delay	t_{CDD}	V_{CC}=2.0V			800	ns	7, 8, 9
		V_{CC}=5V			200		
CLK Low Time	t_{CL}	V_{CC}=2.0V	1000			ns	7
		V_{CC}=5V	250				
CLK High Time	t_{CH}	V_{CC}=2.0V	1000			ns	7
		V_{CC}=5V	250				
CLK Frequency	t_{CLK}	V_{CC}=2.0V			0.5	MHz	7
		V_{CC}=5V	DC		2.0		
CLK Rise and Fall	t_R, t_F	V_{CC}=2.0V			2000	ns	
		V_{CC}=5V			500		
$\overline{RST}$ to CLK Setup	t_{CC}	V_{CC}=2.0V	4			µs	7
		V_{CC}=5V	1				
CLK to $\overline{RST}$ Hold	t_{CCH}	V_{CC}=2.0V	240			ns	7
		V_{CC}=5V	60				
$\overline{RST}$ Inactive Time	t_{CWH}	V_{CC}=2.0V	4			µs	7
		V_{CC}=5V	1				
$\overline{RST}$ to I/O High Z	t_{CDZ}	V_{CC}=2.0V			280	ns	7
		V_{CC}=5V			70		
SCLK to I/O High Z	t_{CCZ}	V_{CC}=2.0V			280	ns	7
		V_{CC}=5V			70		

*Unless otherwise noted.

TIMING DIAGRAM: READ DATA TRANSFER Figure 5



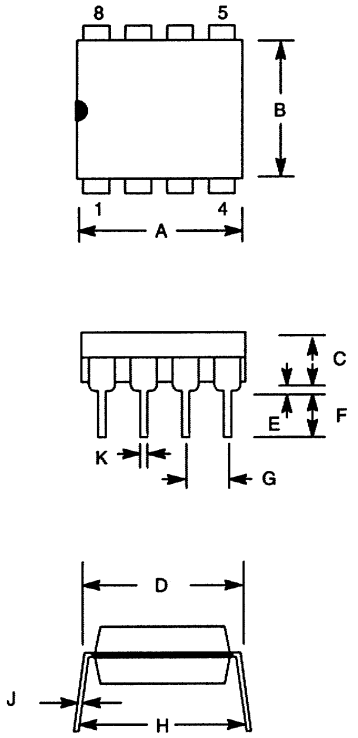
TIMING DIAGRAM: WRITE DATA TRANSFER Figure 6



NOTES:

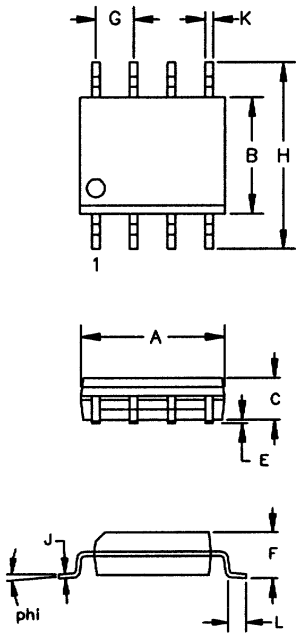
1. All voltages are referenced to ground.
2. Logic one voltages are specified at a source current of 1 mA at V_{CC}=5V and 0.4 mA at V_{CC}=2.0V, V_{OH}=V_{CC} for capacitive loads.
3. Logic zero voltages are specified at a sink current of 4 mA at V_{CC}=5V and 1.5 mA at V_{CC}=2.0V, V_{OL}=GND for capacitive loads.
4. I_{CC1T} and I_{CC2T} are specified with I/O open, $\overline{RST}$ set to a logic "0", and clock halt flag=0 (oscillator enabled).
5. I_{CC1A} and I_{CC2A} are specified with the I/O pin open, $\overline{RST}$ high, SCLK=2 MHz at V_{CC}=5V; SCLK=500 kHz, V_{CC}=2.0V and clock halt flag=0 (oscillator enabled).
6. $\overline{RST}$, SCLK, and I/O all have 40 kΩ pull–down resistors to ground.
7. Measured at V_{IH}=2.0V or V_{IL}=0.8V and 10 ns maximum rise and fall time.
8. Measured at V_{OH}=2.4V or V_{OL}=0.4V.
9. Load capacitance = 50 pF.
10. I_{CC1S} and I_{CC2S} are specified with $\overline{RST}$, I/O, and SCLK open. The clock halt flag must be set to logic one (oscillator disabled).
11. V_{CC}=V_{CC2}, when V_{CC2}>V_{CC1} +0.2V; V_{CC}=V_{CC1}, when V_{CC1}>V_{CC2}.
12. V_{CC2}=0V.
13. V_{CC1}=0V.
14. Typical values are at 25°C.

DS1302 SERIAL TIMEKEEPER 8–PIN DIP (300-MIL)



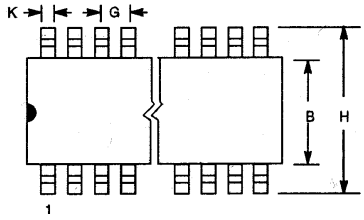
PKG	8-PIN	
DIM	MIN	MAX
A IN.	0.360	0.400
MM	9.14	10.16
B IN.	0.240	0.260
MM	6.10	6.60
C IN.	0.120	0.140
MM	3.05	3.56
D IN.	0.300	0.325
MM	7.62	8.26
E IN.	0.015	0.040
MM	0.38	1.02
F IN.	0.120	0.140
MM	3.04	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.320	0.370
MM	8.13	9.40
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

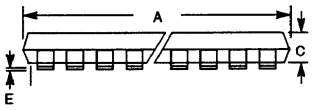
DS1302S SERIAL TIMEKEEPER 8–PIN SOIC (150-MIL AND 200-MIL)

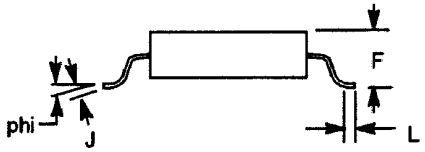


PKG	8-PIN (150 MIL)		8-PIN (200 MIL)	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A IN.	0.188	0.196	0.203	0.213
MM	4.78	4.98	5.16	5.41
B IN.	0.150	0.158	0.203	0.213
MM	3.81	4.01	5.16	5.41
C IN.	0.048	0.062	0.070	0.074
MM	1.22	1.57	1.78	1.88
E IN.	0.004	0.010	0.004	0.010
MM	0.10	0.25	0.10	0.25
F IN.	0.053	0.069	0.074	0.084
MM	1.35	1.75	1.88	2.13
G IN.	0.050 BSC			
MM	1.27 BSC			
H IN.	0.230	0.244	0.302	0.318
MM	5.84	6.20	7.67	8.08
J IN.	0.007	0.011	0.006	0.010
MM	0.18	0.28	0.15	0.25
K IN.	0.012	0.020	0.013	0.020
MM	0.30	0.51	0.33	0.51
L IN.	0.016	0.050	0.019	0.030
MM	0.41	1.27	0.48	0.76
phi	0°	8°	0°	8°

DS1302S SERIAL TIMEKEEPER 16-PIN SOIC







PKG		16-PIN	
DIM		MIN	MAX
A	IN	0.398	0.412
	MM	10.11	10.46
B	IN	0.290	0.300
	MM	7.37	7.62
C	IN	0.089	0.095
	MM	2.26	2.41
E	IN	0.004	0.012
	MM	0.102	0.30
F	IN	0.004	0.105
	MM	2.39	2.67
G	IN	0.050 BSC	
	MM	1.27 BSC	
H	IN	0.398	0.416
	MM	10.11	10.57
J	IN	0.009	0.013
	MM	0.229	0.33
K	IN	0.013	0.020
	MM	0.33	0.51
L	IN	0.016	0.040
	MM	0.40	1.02
phi		0°	8°